UNIVERSAL CURRENT CONVEYOR (UCC) and SECOND-GENERATION CURRENT CONVEYOR (CCII+/-)

UCC FEATURES

- **Wide Bandwidth (40 MHz)**
- **High Slew Rate (53.9 V/µs, 14.7 A/ms)**
- **±0.7 mA Output Current**
- **Four Current Output Terminals**

CCII+/- FEATURES

- **Wide Bandwidth (32 MHz)**
- **High Slew Rate (54.3 V/µs, 30.5 A/ms)**
- **±0.7 mA Output Current**

UCC-N1B FEATURES

- **Supply voltage ±1.65 V**
- **Quiescent current 27 mA**
- **PLCC44 package**

APPLICATIONS

- **Automotive Sensors**
- **Video/Broadcast Equipment**
- **Communications Equipment**
- **Precise Rectification**
- **High-Speed Data Acquisition**
- **Single-ended Frequency Filters**

DESCRIPTION

The UCC-N1B contains the Universal Current Conveyor (UCC) and Second-generation Current Conveyor with positive and negative current outputs (CCII+/-).
The bandwidth of the active

UCC-N1B is made in the CMOS 0.35µm technology with only ±1.65 V supply voltage and quiescent current of 27 mA. For linear operations, maximal output current is up to 700 µA. The voltage transfer of the inner buffers is linear up to 700 mV.

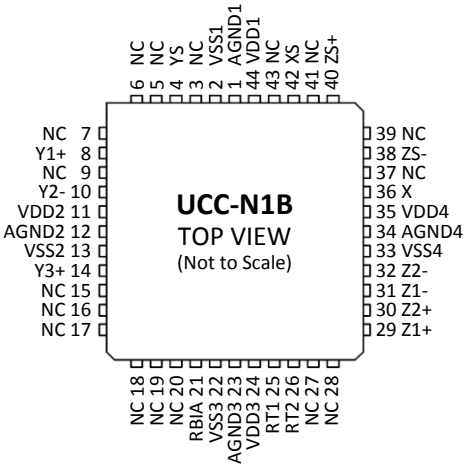


Figure 1. 44-Lead PLCC

PIN CONFIGURATION

Table 1. Pin description of UCC and CCII+/-

Pin	Pin description	Pin	Pin description
4	YS voltage input of CCII+/-	31, 32	Z1-, Z2- negative current outputs of UCC
8	Y1+ positive voltage input of UCC	36	X current input of UCC
10	Y2- negative voltage input of UCC	38	ZS- negative current output of CCII+/-
14	Y3+ positive voltage input of UCC	40	ZS+ positive current output of CCII+/-
29, 30	Z1+, Z2+ positive current outputs of UCC	42	XS current input of CCII+/-

Table 2. Pin description of UCC-N1B (auxiliary pins)

Pin	Pin description	Pin	Pin description
1, 12, 23, 34	AGND Analog ground	21	RBIA Biasing resistor
2, 13, 22, 33	VSS Negative supply voltage	25, 26	RT1, RT2 Offset
11, 34, 35, 44	VDD Positive supply voltage		

SPECIFICATIONS

Vs=±1.65 V, T_A = 25°C, unless otherwise noted

Table 3. Specification of UCC

Parameter	Symbol	Min	Typ	Max	Unit
DC voltage transfers					
V_X/V_{Y1+}	α_1		0.975		[-]
V_X/V_{Y2-}	α_2		0.968		[-]
V_X/V_{Y3+}	α_3		1.009		[-]
Maximal negative input voltage	V_{Y_MAXneg}			-0.73	[V]
Maximal positive input voltage	V_{Y_MAXpos}			0.77	[V]
DC Current transfers					
I_{Z1+}/I_X	γ_{11}		0.965		[-]
I_{Z2+}/I_X	γ_{12}		0.973		[-]
I_{Z1-}/I_X	γ_{21}		1.029		[-]
I_{Z2-}/I_X	γ_{22}		1.023		[-]
Maximal negative input current	I_{X_MAXneg}			-0.64	[mA]
Maximal positive input current	I_{X_MAXpos}			0.64	[mA]
Voltage transfer bandwidth					
V_X/V_{Y1+}	$f_{-3dB-\alpha1}$		40		[MHz]
V_X/V_{Y2-}	$f_{-3dB-\alpha2}$		46		[MHz]
V_X/V_{Y3+}	$f_{-3dB-\alpha3}$		44		[MHz]
Current transfer bandwidth					
I_{Z1+}/I_X	$f_{-3dB-\gamma11}$		43		[MHz]
I_{Z2+}/I_X	$f_{-3dB-\gamma12}$		46		[MHz]
I_{Z1-}/I_X	$f_{-3dB-\gamma21}$		49		[MHz]
I_{Z2-}/I_X	$f_{-3dB-\gamma22}$		48		[MHz]
Voltage slew-rate					
V_X/V_{Y1+}	SR_{Y1+}		53.9		[V/µs]
V_X/V_{Y2-}	SR_{Y2-}		-54.1		[V/µs]
V_X/V_{Y3+}	SR_{Y3+}		54.3		[V/µs]

Table 3. Specification of UCC - continuing

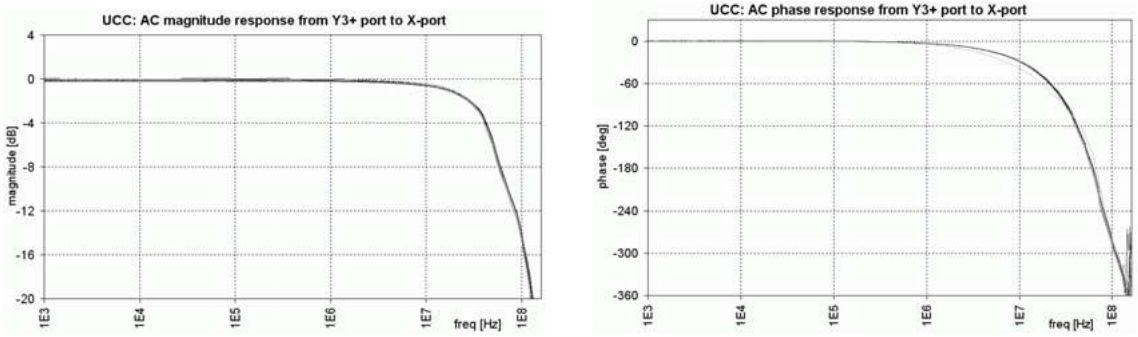
Parameter	Symbol	Min	Typ	Max	Unit
Current slew-rate					
I_{Z1+}/I_X	SR_{Z1+}	12.9			[A/ms]
I_{Z2+}/I_X	SR_{Z2+}	12.3			[A/ms]
I_{Z1-}/I_X	SR_{Z1-}	-13.9			[A/ms]
I_{Z2-}/I_X	SR_{Z2-}	-11.7			[A/ms]
Terminal impedances					
Y1+ terminal	$R_{Y1+}\|\|C_{Y1+}$		348||4.9		[MΩ||pF]
Y2- terminal	$R_{Y2-}\|\|C_{Y2-}$		355||4.5		[MΩ||pF]
Y3+ terminal	$R_{Y3+}\|\|C_{Y3+}$		644||3.9		[MΩ||pF]
X terminal	$R_X + L_X$		2.4+2.9		[Ω+nH]
Z1+ terminal	$R_{Z1+}\|\|C_{Z1+}$		702||5.3		[kΩ||pF]
Z2+ terminal	$R_{Z2+}\|\|C_{Z2+}$		960||4.6		[kΩ||pF]
Z1- terminal	$R_{Z1-}\|\|C_{Z1-}$		847||6.7		[kΩ||pF]
Z2- terminal	$R_{Z2-}\|\|C_{Z2-}$		1.4||4.3		[MΩ||pF]

Table 4. Specification of CCII+/-

Parameter	Symbol	Min	Typ	Max	Unit
DC voltage transfer V_{XS}/V_{YS}	α_S		0.999		[-]
Maximal negative input voltage	V_{YS_MAXneg}			-1.40	[V]
Maximal positive input voltage	V_{YS_MAXpos}			1.25	[V]
DC Current transfers					
I_{ZS+}/I_{XS}	γ_{1S}		0.985		[-]
I_{ZS-}/I_{XS}	γ_{2S}		1.043		[-]
Maximal negative input current	I_{XS_MAXneg}			-0.64	[mA]
Maximal positive input current	I_{XS_MAXpos}			0.67	[mA]
Voltage transfer bandwidth V_{XS}/V_{YS}	$f_{-3dB-\alpha S}$	32			[MHz]
Current transfer bandwidth					
I_{ZS+}/I_{XS}	$f_{-3dB-\gamma 1S}$	45			[MHz]
I_{ZS-}/I_{XS}	$f_{-3dB-\gamma 2S}$	48			[MHz]
Voltage slew-rate V_{XS}/V_{YS}	SR_{YS}	54.3			[V/µs]
Current slew-rate					
I_{ZS+}/I_{XS}	SR_{ZS+}	31.2			[A/ms]
I_{ZS-}/I_{XS}	SR_{ZS-}	-30.5			[A/ms]
Terminal impedances					
YS terminal	$R_{YS}\|\|C_{YS}$		88||4.6		[MΩ||pF]
XS terminal	$R_{XS} + L_{XS}$		1.8+1.4		[Ω+uH]
ZS+ terminal	$R_{ZS+}\|\|C_{ZS+}$		1.1||2.7		[MΩ||pF]
ZS- terminal	$R_{ZS-}\|\|C_{ZS-}$		1.2||3.6		[MΩ||pF]

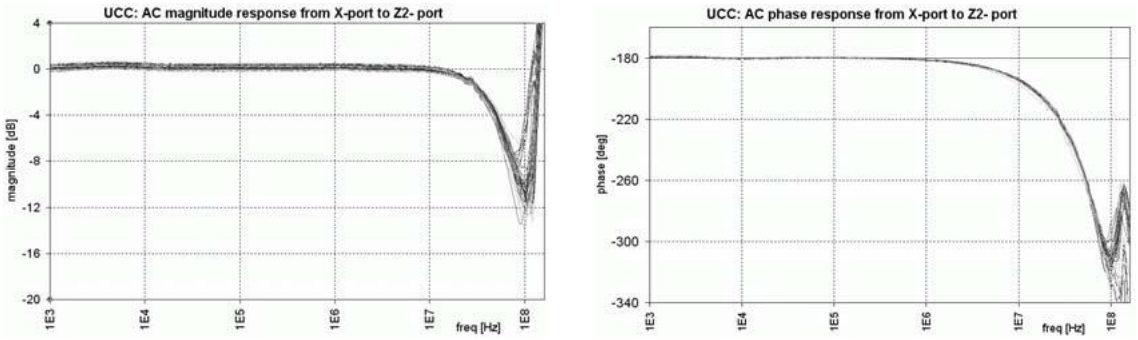
TYPICAL AC and DC CHARACTERISTICS of UCC: V_S = ± 1.65 V

R_{XL} = 1 MΩ, R_{ZL} = 10 Ω, T_A = 25°C, unless otherwise noted



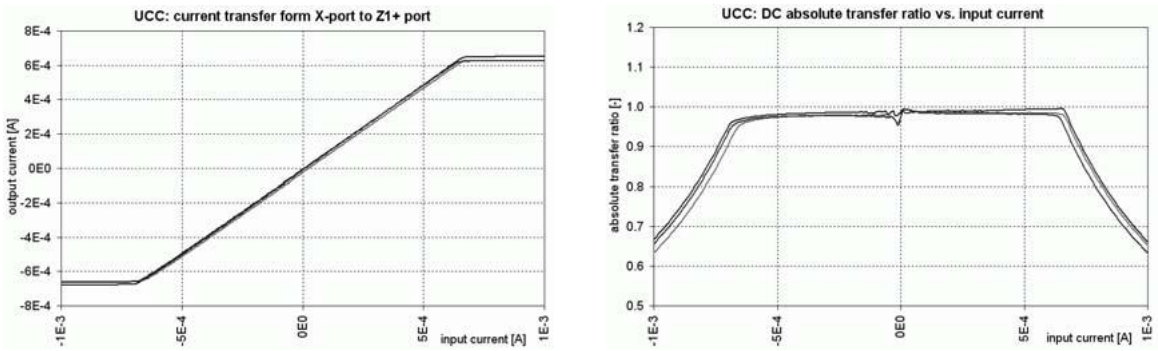
(a) (b)

Figure 2. (a) Magnitude and (b) Phase of the Voltage transfer V_X/V_{Y3+}



(a) (b)

Figure 3. (a) Magnitude and (b) Phase of the Current transfer I_{Z2-}/I_X

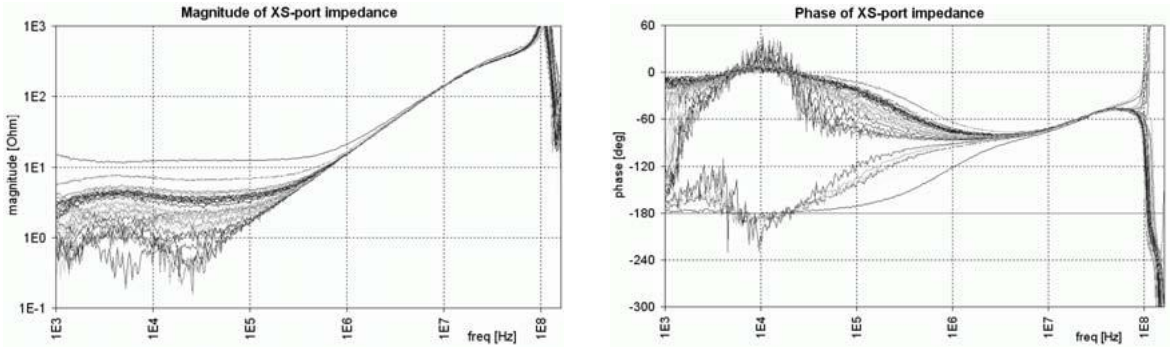


(a) (b)

Figure 4. (a) DC Current transfer I_{Z1+}/I_X and (b) Absolute transfer ratio dependency on input current of the Current transfer I_{Z1+}/I_X

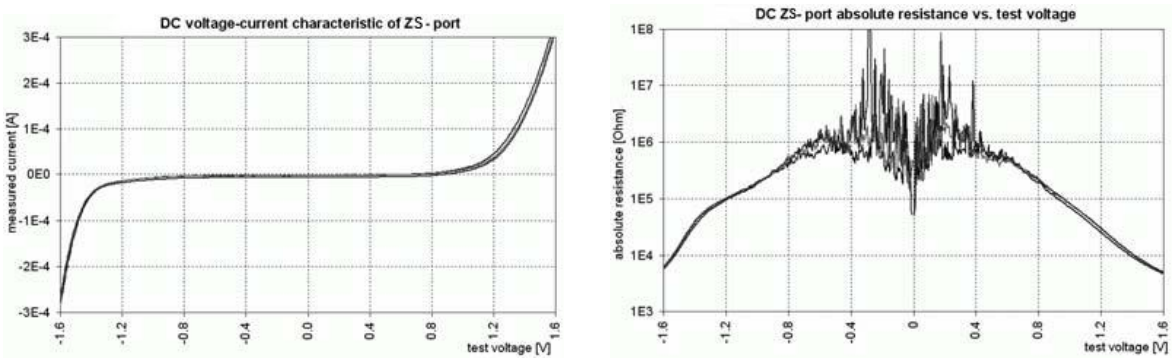
TYPICAL AC and DC CHARACTERISTICS of CCII+/-: V_S = ± 1.65 V

R_{XSL} = 1 MΩ, R_{ZSL} = 10 Ω, T_A = 25°C, unless otherwise noted



(a) (b)

Figure 5. (a) Magnitude and (b) Phase of the XS terminal



(a) (b)

Figure 6. (a) DC Voltage-Current characteristic of ZS- terminal and (b) absolute resistance dependency on test voltage

BASIC CONNECTION AND AUXILIARY CIRCUITRY

The UCC-N1B is supplied by ±1.65 V voltage. For proper operation, bypass capacitors C_{B1}-C_{B6} are required (Figure 7). The C_{B1}-C_{B4} is a parallel combination of NPO capacitors with values of 68 pF and 47 nF. The C_{B5} and C_{B6} are 4u7 tantalum capacitors.

An external resistor R_{BIA} = 4.7 kΩ is used for biasing the active element. For offset cancelation of the UCC the trimmer R_T can be used.

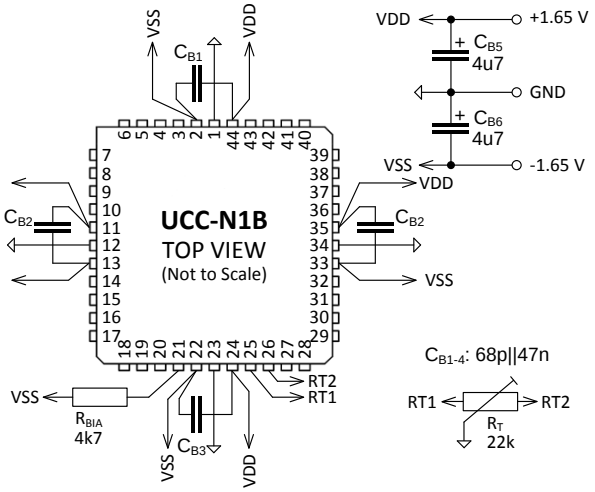


Figure 7 Auxiliary circuitry of UCC-N1B

UCC and CCII+/- DESCRIPTION

The UCC is an 8-port active element described as:

$$V_X = \alpha_1 V_{Y1} - \alpha_2 V_{Y2} + \alpha_3 V_{Y3}$$

$$I_{Z1+} = \gamma_{11} I_X,\ I_{Z2+} = \gamma_{12} I_X$$

$$I_{Z2-} = -\gamma_{21} I_X,\ I_{Z2-} = -\gamma_{22} I_X.$$

The currents into the Y-terminals are assumed to be zero and the voltages at Z-terminals are generally not defined by the UCC, but by the impedances connected.

The advantage of the UCC is in the possibility of replacing a family of current conveyors with one current input, i.e. one terminal X. By simple interconnection and grounding of appropriate terminals of UCC 32 different current conveyors can be described, as listed in Table 5. Furthermore, the universality of the UCC is its use for the design of Balanced-output Operational Transconductance Amplifier (BOTA), or a Four-Terminal Floating Nullor (FTFN), see Figure 10.

The CCII+/- is a 4-port active element with two current outputs and its behavior is described as follows:

$$V_{XS} = \alpha_S V_{YS},\ I_{ZS+} = \gamma_{1S} I_{XS},\ I_{ZS-} = -\gamma_{2S} I_{XS}.$$

Also here current into Y-terminal is zero and voltage at Z-terminals is not defined by the CCII+/-.

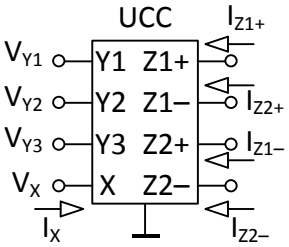


Figure 8. Electrical symbol and terminal voltages and currents of the Universal Current Conveyor

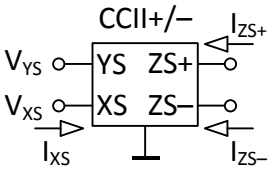
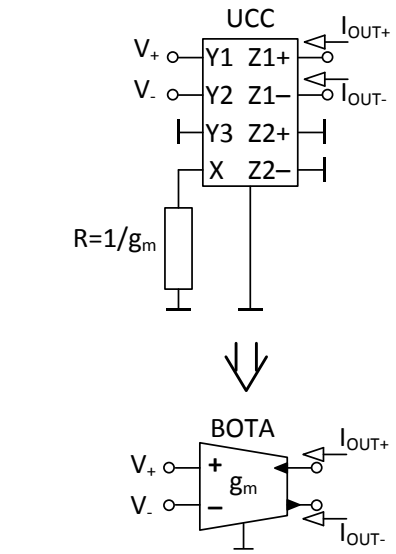
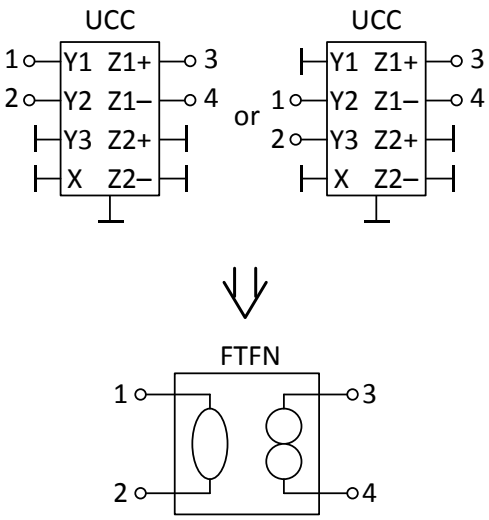


Figure 9. Electrical symbol and terminal voltages and currents of the Second-Generation Current Conveyor



(a)



(b)

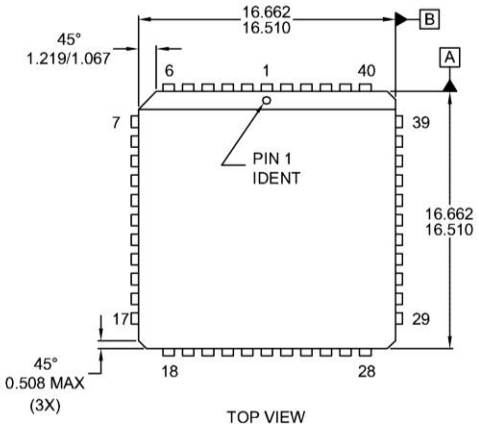
Figure 10. Realization of (a) BOTA and (b) FTFN using UCC

Table 5. Current Conveyors realized by the UCC

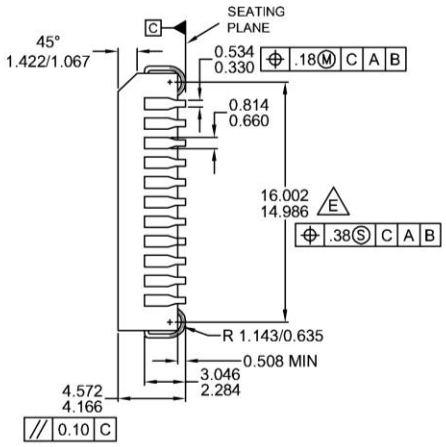
Type	Input	Output	Interconnected	Grounded
CCI+	Y1 input Y	Z2+ output Z	Y1 and Z1+	Y2, Y3, Z1–, Z2–
CCI-	Y1 input Y	Z1– output Z	Y1 and Z1+	Y2,Y3, Z2+, Z2–
CCI+/-	Y1 input Y	Z2+ output Z, Z1– output Z–	Y1 and Z1+	Y2, Y3, Z2–
CCI-/-	Y1 input Y	Z1– output Z1, Z2– output Z2	Y1 and Z1+	Y2, Y3
CCII+	Y1 input Y	Z1+ output Z		Y2, Y3, Z2+, Z1–, Z2–
CCII-	Y1 input Y	Z1- output Z		Y2, Y3, Z1+, Z2+, Z2–
CCII+/-	Y1 input Y	Z1+ output Z, Z1– output Z-		Y2, Y3, Z2+, Z2–
CCII+/+	Y1 input Y	Z1+ output Z1, Z2+ output Z2		Y2, Y3, Z1–, Z2–
CCII-/-	Y1 input Y	Z1– output Z1, Z2– output Z2		Y2, Y3, Z1+, Z2+
CCIII+	Y1 input Y	Z1+ output Z	Y1 and Z1–	Y2, Y3, Z2+, Z2–
CCIII-	Y1 input Y	Z2– output Z	Y1 and Z1–	Y2, Y3, Z1+, Z2+
CCIII+/-	Y1 input Y	Z1+ output Z, Z2– output Z	Y1 and Z1–	Y2, Y3, Z2+
CCIII+/+	Y1 input Y	Z1+ output Z1, Z2+ output Z2	Y1 and Z1–	Y2, Y3, Z2–
ICCI+	Y2 input Y	Z2+ output Z	Y2 and Z1+	Y1, Y3, Z1–, Z2–
ICCI-	Y2 input Y	Z1– output Z	Y2 and Z1+	Y1,Y3, Z2+, Z2–
ICCI+/-	Y2 input Y	Z2+ output Z, Z1– output Z–	Y2 and Z1+	Y1, Y3, Z2–
ICCI-/-	Y2 input Y	Z1– output Z1, Z2– output Z2	Y2 and Z1+	Y1, Y3
ICCII+	Y2 input Y	Z1+ output Z		Y2, Y3, Z2+, Z1–, Z2–
ICCII-	Y2 input Y	Z1– output Z		Y2, Y3, Z1+, Z2+, Z2–
ICCII+/-	Y2 input Y	Z1+ output Z, Z1– output Z–		Y2, Y3, Z2+, Z2–
ICCII+/+	Y2 input Y	Z1+ output Z1, Z2+ output Z2		Y2, Y3, Z1–, Z2–
ICCII-/-	Y2 input Y	Z1– output Z1, Z2– output Z2		Y2, Y3, Z1+, Z2+
ICCIII+	Y2 input Y	Z1+ output Z	Y2 and Z1–	Y1, Y3, Z2+, Z2–
ICCIII-	Y2 input Y	Z2– output Z	Y2 and Z1–	Y1, Y3, Z1+, Z2+
ICCIII+/-	Y2 input Y	Z1+ output Z, Z2– output Z–	Y2 and Z1–	Y1, Y3, Z2+
ICCIII+/+	Y2 input Y	Z1+ output Z1, Z2 – output Z2	Y2 and Z1–	Y1, Y3, Z2–
DVCCI-	Y1 input Y1 Y2 input Y2	Z1– output Z	Y1 and Z1+, Y2 and Z2+	Y3, Z2–
DVCC	Y1 input Y1 Y2 input Y2	Z1+ output Z1, Z1– output Z2		Y3, Z2+, Z2–
DVCCIII+	Y1 input Y1 Y2 input Y2	Z1+ output Z	Y1 and Z1–, Y2 and Z2-	Y3, Z2+
DDCC+	Y1 input Y1 Y2 input Y2 Y3 input Y3	Z1+ output Z		Z2+, Z1–, Z2–
DDCC-	Y1 input Y1 Y2 input Y2 Y3 input Y3	Z1– output Z		Z1+, Z2+, Z2–
DDCC+/-	Y1 input Y1 Y2 input Y2 Y3 input Y3	Z1+ output Z1, Z1– output Z2		Z2+, Z2–

PACKAGE INFORMATION

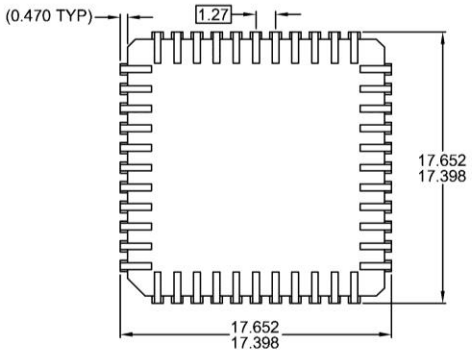
44-pin PLCC



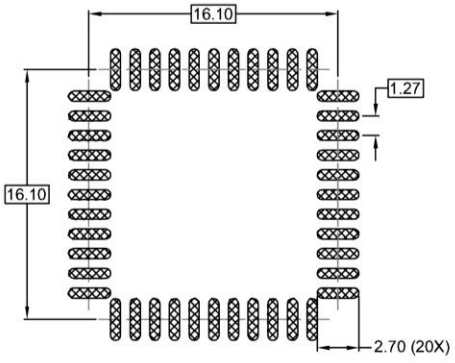
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)

NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC MS-018, VARIATION AC.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
E. MEASURED AT SEATING PLANE (DATUM C) CONTACT POINT.
F. LAND PATTERN STANDARD: PLCC127P1752X1752X457-44M.